

December 10, 1999

**Box Patent Application**

Assistant Commissioner for Patents  
Washington, D. C. 20231

Enclosed herewith for filing is a patent application, as follows:

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Wei-Bing Chu

Title: Semiconductor Die Package Including Cup-Shaped Leadframe

<u>X</u>	<u>Return Receipt Postcard</u>
<u>X</u>	This Transmittal Letter (in duplicate)
<u>4</u>	page(s) Specification (not including claims)
<u>1</u>	page(s) Claims (Figs. 1-7)
<u>1</u>	page Abstract
<u>3</u>	page(s) Declaration For Patent Application and Power of Attorney (Unsigned)
<u>1</u>	Sheet(s) of Drawings

**CLAIMS AS FILED (fees computed under §1.9(f))**

For	Number Filed		Number Extra		Rate		Basic Fee
Total Claims	8	-20 =	0	x	\$18.00	=	\$ 760.00
Independent Claims	1	-3 =	0	x	\$78.00	=	\$ 0.00
<input type="checkbox"/> Application contains one or more multiple dependent claims ( total fee)							\$
<input type="checkbox"/> Fee for Request for Extension of Time							\$

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09/468249

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- 1 -

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When the package is mounted on, for example, a printed circuit board (PCB), the first electrical terminal is electrically connected to the PCB via the leadframe. The second electrical terminal is connected to the PCB directly using solder or another conductive material.

- 5       The package is particularly suitable for use with power MOSFETs which require a contact to the backside (drain) terminal, but it can also be used with any integrated circuit die where contact must be made to both sides of the die.

The package of this invention is easy to manufacture and can be made very thin (i.e., less than 1 mm thick).

#### 10       BRIEF DESCRIPTION OF THE DRAWINGS

**Fig. 1** shows a cross-sectional view of a semiconductor package in accordance with this invention.

**Fig. 2** shows a bottom view of the semiconductor package.

**Fig. 3** shows a top view of the semiconductor package.

- 15       **Fig. 4** shows an end view of the semiconductor package.

**Fig. 5** is a flow chart of a process for manufacturing the semiconductor package.

**Fig. 6** is a cross-sectional view of an alternative embodiment of the invention.

- 20       **Fig. 7** is a bottom view of a package for an integrated circuit die in accordance with this invention.

#### DESCRIPTION OF THE INVENTION

- Fig. 1** shows a cross-sectional view of a semiconductor package 10 in accordance with this invention. Semiconductor package 10 includes a
- 25       semiconductor die 12 and a leadframe 14, which is preformed in the shape of a cup. The die 12, which in this embodiment contains a vertical MOSFET, is located inside the “cup”. One side of die 12 (the backside) contains a drain terminal (not shown), which is electrically connected to leadframe 14 by means of a layer 16 of conductive epoxy or another type of conductive cement. Each of the individual
- 30       leads 19 of leadframe 14 includes a portion 18 that is coplanar with the second side of the die 12. A capsule 20 made of a plastic material is in contact with the outside of the “cup”, and a portion 22 of the plastic material is injected into a region inside

the “cup” between the edge of die 12 and leadframe 14. The molding process used in the manufacture of package 10 ensures that the frontside of die 12 is left uncovered by the plastic material.

5 **Fig. 1** is taken at cross-section I-I shown in **Fig. 3**, which is a top view of semiconductor package 10. As shown, package 10 has a length X which could be 240 mils and a width Y which could be 200 mils. Die 12 is shown in dashed lines in **Fig. 3**. As shown in **Fig. 1**, package 10 has a thickness Z that can be 0.7 mm or less.

10 **Fig. 2** shows a view of package 10 from the bottom. The bottom (frontside) of die 12 contains a gate terminal 24 and four source terminals 26 which surround gate terminal 24.

**Fig. 4** shows an end view of semiconductor package 10, taken from direction 30 shown in **Fig. 3**.

15 **Fig. 5** shows a flow chart for a process of manufacturing the semiconductor package. The process begins with the step of sawing a semiconductor wafer into individual dice. The dice are attached to leadframes (L/F) using, for example, a conductive epoxy 84-1 produced by Ablestik Electronic Materials and Adhesives. The leadframes are preformed into cup shapes as described above, with each cup having dimensions (width, length and depth) suitable to hold one of the dice.  
20 Preformed leadframes are available from many sources known to those skilled in the art.

Using a conventional injection-molding machine, plastic capsules are formed around the leadframes and dice, without touching the frontside of the die 12. Holes may be formed in the leadframe to allow the plastic material to fill the spaces between the edges of the dice and the leadframes (e.g., portion 22 in **Figs. 1** and **2**). The plastic material may be the thermal set plastic 6300H, supplied by Sumitomo of Japan.  
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Next, the packages are marked, and the leadframes are separated by cutting the leads (a process sometimes referred to as “singulation”). Finally, the dice can  
30 be subjected to electrical tests to ensure that they are fully operational.

Since the frontside of the die and the leads are coplanar, the package may easily be mounted on the surface of a PCB, as shown in **Fig. 1**.

The package of this invention is economical to manufacture and provides a electrical contacts to both sides of a dice. In addition, the direct connection between the die and the PCB provides a good thermal conduction path from the die to the PCB.

5           Alternatively, the package can be formed as shown in the cross-sectional view of **Fig. 6**. In package 30 the capsule 32 is truncated, leaving the top of the leadframe is exposed. This embodiment may further improve the thermal dissipation properties of the package.

10           While this invention was described with reference to a vertical MOSFET, this description is to be considered illustrative and not limiting. The broad principles of this invention are applicable to any semiconductor die which is to be packaged in such a way that contact is made to both sides of the die, including integrated circuit (IC) dice that require a contact to the frontside. For example, **Fig. 7** shows a bottom view of an package 40 which includes an IC die 42. Ten  
15           input/output (I/O) pads 44 are located on the frontside of IC die 42. **Fig. 7** is similar to **Fig. 2**, with a cup-shaped leadframe being electrically connected to the backside of die 42 (typically ground) and having leads with portions 46 (similar to portions 18) that are coplanar with the frontside of die 42.

20           Persons skilled in the art will appreciate that numerous other embodiments may be fabricated in accordance with the broad principles of this invention.

CLAIMS

We claim:

1. A semiconductor package comprising:
  - a semiconductor die having first and second sides, a first electrical terminal being located on the first side, at least a second electrical terminal being located on the second side; and
  - a leadframe in electrical contact with the first terminal, the leadframe being formed in the shape of a cup, the die being located in the cup, at least one lead of the leadframe containing a portion that is coplanar with the second side of the die.
2. The semiconductor package of Claim 1 further comprising a layer of conductive cement located inside the cup between the first terminal and the leadframe.
3. The semiconductor package of Claim 2 wherein the conductive cement comprises conductive epoxy.
4. The semiconductor package of Claim 1 further comprising a plastic capsule in contact with an outside of the cup.
5. The semiconductor package of Claim 4 wherein the die is in electrical contact with a bottom of the cup, an outside of the bottom of the cup being exposed.
6. The semiconductor package of Claim 1 further comprising a plastic material located inside the cup between an edge of the die and the leadframe.
7. The semiconductor package of Claim 1 wherein the semiconductor die comprises a MOSFET.
8. The semiconductor package of Claim 1 wherein the semiconductor die comprises an integrated circuit.

SEMICONDUCTOR DIE PACKAGE  
INCLUDING CUP-SHAPED LEADFRAME

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King Owyang

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Yueh-Se Ho

Y. Mohammed Kasem

Lixiong Luo

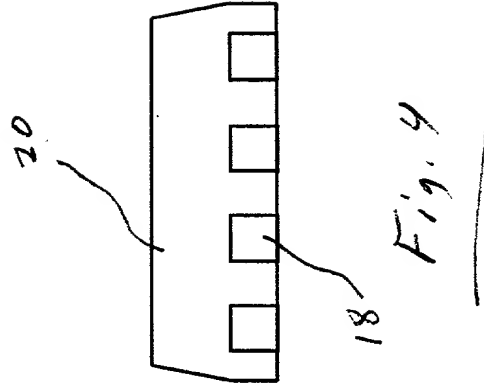
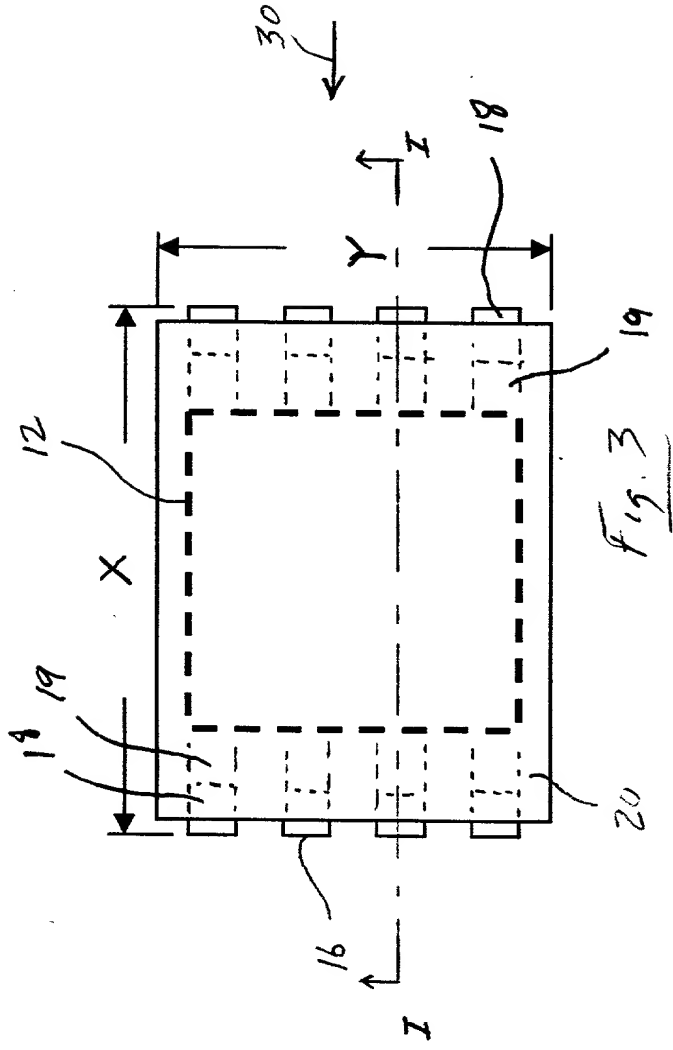
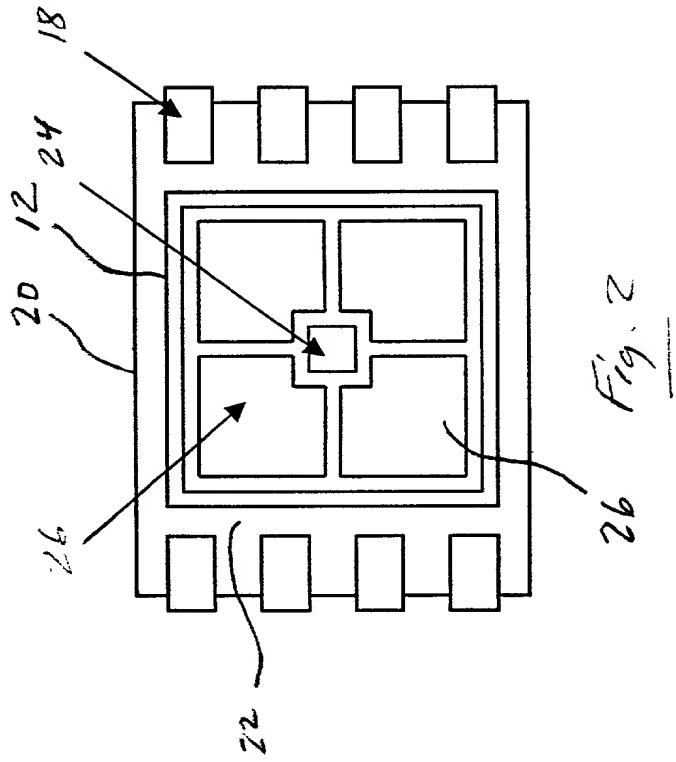
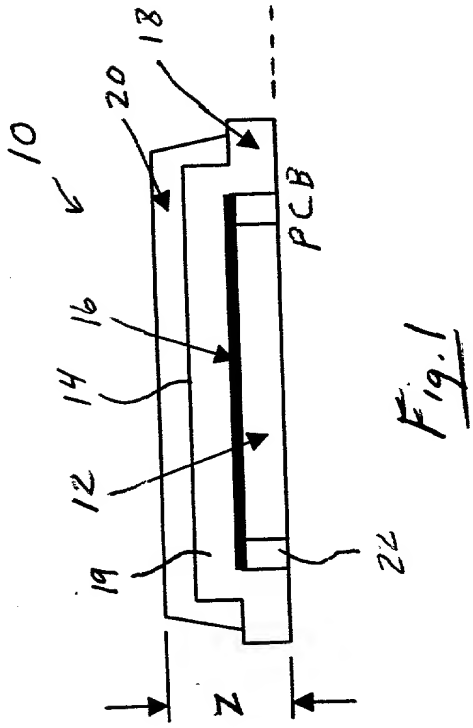
Wei-Bing Chu

ABSTRACT

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A semiconductor package includes a leadframe which is cup-shaped and holds a semiconductor die. The leadframe is in electrical contact with a terminal on one side of the die, and the leads of the leadframe are bent in such a way that portions of the leads are coplanar with the other side of the die, which also contains one or more terminals. A plastic capsule is formed around the leadframe and die.

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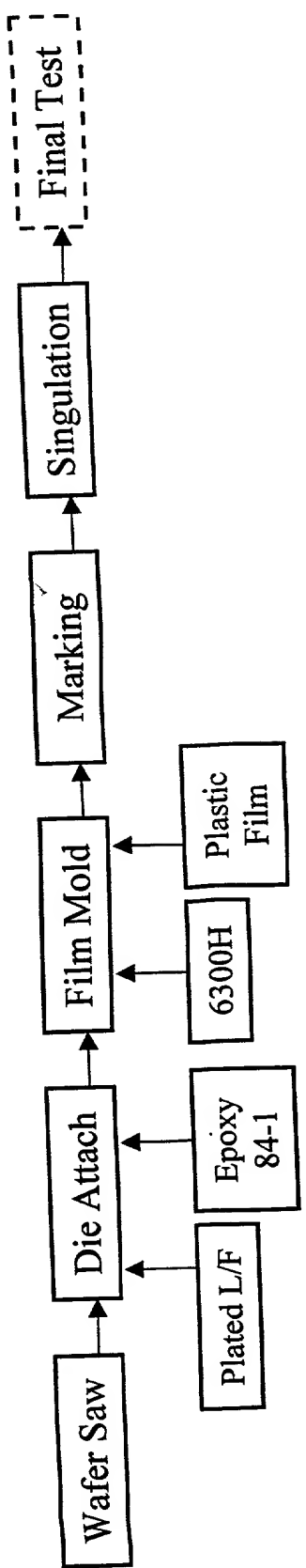


Fig. 5

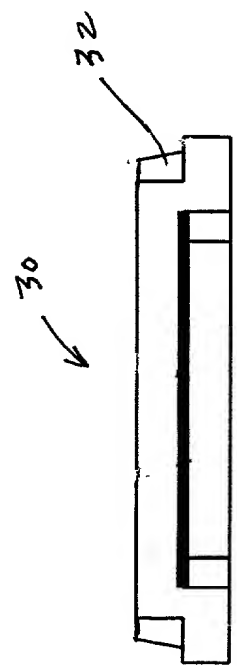


Fig. 6

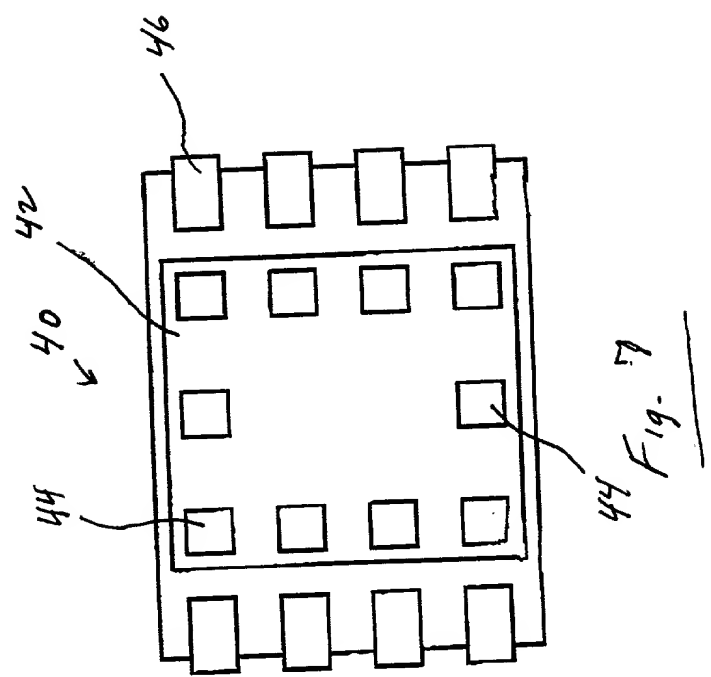


Fig. 7

**DECLARATION FOR PATENT APPLICATION  
AND POWER OF ATTORNEY**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

**Semiconductor Die Package Including Cup-Shaped Leadframe**

which (check) ☒ is attached hereto.  
☐ and is amended by the Preliminary Amendment attached hereto.  
☐ was filed on \_\_\_\_\_ as Application Serial No.  
☐ and was amended on \_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			<input type="checkbox"/>	<input type="checkbox"/>

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

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